Embedded System Design Challenges
Definition and Significance
System-on-Chip Today
Main Challenges on Design
Some Answers
Overview of the Course
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Overview of the Course
Definition
What is an embedded system?

- **system**
  - set of components needed to perform a function
  - hardware + software + ...

- **embedded**
  - main function *not computing*
  - usually not autonomous

- usually
  - computer inside a system
  - *specific purpose*
  - submitted to *constraints*
Examples

- very small
  - electronic tags
  - smartcards
- microcontrollers
  - washing machine, microwave oven, ...
  - computer peripherals
    - keyboard
    - hard drive controller
- more complex controllers
  - digital camera
  - automotive
    - air bags, ABS, ...
    - ESB, engine control, ...
Examples – continued

- communications
  - mobile phones
  - network routers, modems
  - software radio
- multimedia
  - set-top boxes
    - cable, satellite TV
    - HDTV, DVD players
  - video games
- radar, sonar
Market Significance

- huge market
  - estimation 2002 (VDC) : > 1.7 billion units
  - estimation 2003 (VDC) : $760 million for embedded software
  - number of HW and SW developers increases

- becomes more important than general purpose computing
  - number of units
    - already
  - number of developers
    - in a few years
The metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry quickly tends to make obsolete many portions of the ORTC metrics and, consequently, the roadmap. Hopefully, the gathering and analysis of actual data, combined with the ITRS annual update process, will provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS for the industry.

For example, the actual data and conference papers, along with company survey data and public announcements will be re-evaluated during the year 2004 ITRS update process, and the possibility of a continued two-year node cycle. In addition, logic and Flash product half-pitch acceleration will be monitored for future leadership candidates.

As mentioned above, to reflect the variety of cycles and to allow for closer monitoring of future roadmap shifts, it was agreed to continue the practice of publishing annual technology requirements from 2003 through 2009, called the "Near-term Years," and at three-year (node) intervals thereafter, called the "Long-term Years" (2012, 2015, 2018), while retaining the previous 2001 ITRS long-term columns for ease of comparison and to retain the tracking of the three-year cycle nodes.
Table 1i  High-Performance MPU and ASIC Product Generations and Chip Size Model—Near-term Years

<table>
<thead>
<tr>
<th>Year of Production</th>
<th>2003</th>
<th>2004</th>
<th>2005</th>
<th>2006</th>
<th>2007</th>
<th>2008</th>
<th>2009</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology Node</td>
<td>hp90</td>
<td></td>
<td></td>
<td></td>
<td>hp65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>DRAM ½ Pitch (nm)</td>
<td>100</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
</tr>
<tr>
<td>MPU/ASIC Metal 1 (M1) ½ Pitch (nm)</td>
<td>120</td>
<td>107</td>
<td>95</td>
<td>85</td>
<td>76</td>
<td>67</td>
<td>60</td>
</tr>
<tr>
<td>MPU/ASIC ½ Pitch (nm) (Un-contacted Poly)</td>
<td>107</td>
<td>90</td>
<td>80</td>
<td>70</td>
<td>65</td>
<td>57</td>
<td>50</td>
</tr>
<tr>
<td>MPU Printed Gate Length (nm) ††</td>
<td>65</td>
<td>53</td>
<td>45</td>
<td>40</td>
<td>35</td>
<td>32</td>
<td>28</td>
</tr>
<tr>
<td>MPU Physical Gate Length (nm)</td>
<td>45</td>
<td>37</td>
<td>32</td>
<td>28</td>
<td>25</td>
<td>22</td>
<td>20</td>
</tr>
<tr>
<td>Logic (Low-volume Microprocessor) High-performance ‡</td>
<td>p03h</td>
<td>--</td>
<td>p05h</td>
<td>--</td>
<td>p07h</td>
<td>--</td>
<td>p09h</td>
</tr>
<tr>
<td>Functions per chip (million transistors)</td>
<td>439</td>
<td>553</td>
<td>697</td>
<td>878</td>
<td>1,106</td>
<td>1,393</td>
<td>1,756</td>
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<tr>
<td>Chip size at production (mm$^2$) §§</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
<td>310</td>
</tr>
<tr>
<td>High-performance MPU Mtransistors/cm$^2$ at production (including on-chip SRAM) ‡</td>
<td>142</td>
<td>178</td>
<td>225</td>
<td>283</td>
<td>357</td>
<td>449</td>
<td>566</td>
</tr>
<tr>
<td>ASIC</td>
<td></td>
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<tr>
<td>ASIC usable Mtransistors/cm$^2$ (auto layout)</td>
<td>142</td>
<td>178</td>
<td>225</td>
<td>283</td>
<td>357</td>
<td>449</td>
<td>566</td>
</tr>
<tr>
<td>ASIC max chip size at production (mm$^2$) (maximum lithographic field size)</td>
<td>572</td>
<td>572</td>
<td>572</td>
<td>572</td>
<td>572</td>
<td>572</td>
<td>572</td>
</tr>
<tr>
<td>ASIC maximum functions per chip at production (Mtransistors/chip) (fit in maximum lithographic field size)</td>
<td>810</td>
<td>1,020</td>
<td>1,286</td>
<td>1,620</td>
<td>2,041</td>
<td>2,571</td>
<td>3,239</td>
</tr>
</tbody>
</table>
Today, we have the opportunity to define a reuse strategy that can not only co-exist for FPGAs and ASICs but can also work seamlessly between the two technologies. The decision to include FPGAs in a Design Reuse strategy must be made upfront because it affects almost all phases of the Design Reuse process, from design specification to verification planning.

Sharing RTL Design Methods

One of the most exciting outcomes of the dramatic improvements in FPGA architectures, pricing, and design tools is that this technology advancement has made it possible for ASIC and FPGA designers to share a common RTL design methodology. A common RTL design methodology is the basis for a common design reuse methodology. Though ASICs will continue to provide higher levels of design integration, higher speeds, and new EDA environments, FPGAs are never far behind. The major FPGA and EDA companies have made a conscious decision to keep their design environments the same, from the end users point of view, to make it easy for users to move from one technology to the another. This was illustrated by the wide adoption of RTL synthesis tools and verification tools in the mid-1990s. In the case of RTL synthesis, existing ASIC methodology was kept the same and the synthesis algorithms were changed to target specific FPGA devices. Today we are seeing higher-level EDA tools such as Floorplanners and team-based design tools using the Internet.

Conclusion

In 1999, the number of ASIC design starts peaked at only 1000 designs, and despite all the publicity over the multimillion gates designs, most of these design starts were under 200K transistors. The average FPGA design start in 1999 was between 10K and 50K gates, with the fastest growing size range between 50K and 100K gates. Considering that FPGAs are more widely used than ASICs in digital designs today, it makes sense to include FPGAs in a design reuse strategy. There are many benefits of sharing a common design reuse strategy; one of the most compelling is the flexibility it gives the designer to choose the IC technology late in the design cycle. It provides the flexibility to choose the best method to implement an SLI design without the overhead of retraining the design teams. In this fast pace market it is difficult to predict what features your product will need and what technology you should use.

A Design Reuse strategy is more than RTL code and synthesis. Many companies reusing designs have found more value in the design and test specifications than the actual RTL design. If you are currently an ASIC user, the good news is that many of the elements of a good design reuse methodology can easily incorporate FPGAs with minimal modifications.

Xilinx has joined efforts with Qualis Design Corporation to create the first Reuse Design Guide for FPGA users. This new FPGA Reuse Field Guide will walk you through the elements of building a design reuse strategy and is available, free of charge, from the Xilinx website at: www.xilinx.com/ipcenter.
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Some Answers

Overview of the Course
System-on-Chip

- definition
  - (nearly) complete embedded system
  - on a single chip
- usually includes
  - *programmable processors*
  - *memory*
  - *accelerating function units*
  - *I/O*
  - *software*
Technology Integration

<table>
<thead>
<tr>
<th>Technology</th>
<th>98</th>
<th>99</th>
<th>00</th>
<th>01</th>
<th>02</th>
<th>03</th>
<th>04</th>
<th>06</th>
<th>08</th>
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<tbody>
<tr>
<td>Logic</td>
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<td>SRAM</td>
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<td>Flash</td>
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<td>E-DRAM</td>
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<td>CMOS RF</td>
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<td>FPGA</td>
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<td>FRAM</td>
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<td>MEMS</td>
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<tr>
<td>Chemical sensors</td>
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<tr>
<td>Electro-optical</td>
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<tr>
<td>Electro-biological</td>
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</tbody>
</table>

Figure 9  First Integration of Technologies in SOC with Standard CMOS Process
SoC Examples

- Canon Digic processor family
  - image processor
  - improved quality, power consumption, speed, cost
- STI Cell
  - Sony+Toshiba+IBM
  - aim at several TFlops at 65nm integration
  - one PowerPC + 8 SIMD units
- TI OMAP
  - platform
  - dedicated to 2.5G and 3G mobile phones / PDA
STI Cell

http://www.blachford.info/computer/Cell/Cell0_v2.html
OMAP1612

**Typical application using the OMAP1612 device**

OMAP1612 application processor

For high-performance, space-constrained product platforms, the OMAP1612 application processor includes all the capabilities of the OMAP1611 device plus the added benefit of stacked mobile double data rate (DDR) memory. The significance of DDR memory to system designers is it allows for a 100-MHz interface clock to memory while providing memory access speeds up to 200 MHz. With stacked memory, mobile device manufacturers can design a system with a very small footprint but expanded memory storage. The stacked memory options include up to 256 Mb of storage. In addition, the OMAP1612 processor's stacked memory consumes less power than traditional external memory because of reduced load capacitance on the IOs.
### Table 9  System Functional Requirements for the PDA SOC-LP Driver

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</tr>
</thead>
<tbody>
<tr>
<td>Process Technology (nm)</td>
<td>101</td>
<td>90</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1.2</td>
<td>1</td>
<td>0.8</td>
<td>0.6</td>
<td>0.5</td>
<td>0.4</td>
</tr>
<tr>
<td>Clock Frequency (MHz)</td>
<td>300</td>
<td>450</td>
<td>600</td>
<td>900</td>
<td>1200</td>
<td>1500</td>
</tr>
<tr>
<td>Application (maximum required performance)</td>
<td>Still Image Processing</td>
<td>Real Time Video Codec (MPEG4/CIF)</td>
<td>Real Time Interpretation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Application (other)</td>
<td>Web Browser</td>
<td>TV Telephone (1:1)</td>
<td>TV Telephone (&gt;3:1)</td>
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<tr>
<td></td>
<td>Electric Mailer</td>
<td>Voice Recognition (Input)</td>
<td>Voice Recognition (Operation)</td>
<td></td>
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<tr>
<td></td>
<td>Scheduler</td>
<td>Authentication (Crypto Engine)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Processing Performance (GOPS)</td>
<td>0.3</td>
<td>2</td>
<td>14</td>
<td>77</td>
<td>461</td>
<td>2458</td>
</tr>
<tr>
<td>Required Average Power (W)</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
<td>0.1</td>
</tr>
<tr>
<td>Required Standby Power (mW)</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>Battery Capacity (Wh/Kg)</td>
<td>120</td>
<td>200</td>
<td>200</td>
<td>400</td>
<td>400</td>
<td>400</td>
</tr>
</tbody>
</table>
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Technology Challenges for SoC Design

- **design productivity** increase
  - **main challenge**
  - need >100% increase per technology node
- **management of power**
  - especially for low-power, wireless, multimedia applications
- **system-level integration of heterogeneous technologies**
- **development of SoC test methodology**
Target Design Freedom
100% of Design Productivity Improvement

Figure 13  New and Reused Logic Content versus Memory Content with Constant Die Size and Insufficient (42% Per Node) Design Productivity Growth

Figure 14a  Evolution of Maximum Logic Content with Different Rates of Design Productivity Improvement

Figure 14b  100% Productivity Improvement per Node Will Preserve Designer Freedom at the End of the ITRS Forecast Period
Logic vs Memory
with Different Rates of Productivity Improvement
Figure 13    Impact of Design Technology on SOC LP-P DA Implementation Cost

This chapter first presents silicon complexity and system complexity challenges, followed by five crosscutting challenges (productivity, power, manufacturing integration, interference, and error tolerance) that permeate all DT areas. The bulk of the chapter then sets out detailed challenges according to a traditional landscape of DT areas (see Figure 14): design process; system-level design; logical, circuit, and physical design; design verification; and design test.

These challenges are discussed at a level of detail that is actionable by management, R&D, and academia in the target supplier community, i.e., the electronic design automation (EDA) industry. As appropriate, the detailed challenges are mapped to the MPU, SOC, AMS, and memory system drivers; most challenges map to MPU and SOC, reflecting today’s EDA technology and market segmentation. A brief unified overview of AMS-specific DT is given to reflect the rise of application- and driver-specific DT, and the likely organization of future ITRS Design Chapter editions according to system drivers, rather than traditional areas of DT.

Additional discussion of analog/mixed-signal circuit issues is contained in the System Drivers Chapter (AMS Driver). Test equipment and the test of manufactured chips are discussed in the Test Chapter, while this chapter addresses design for testability, including built-in self-test (BIST).
Design Cost Problem

- economy will limit the semiconductor industry
  - before the end of Moore’s law
- today design time
  - 30% design
  - 70% verification/test
Complexity Challenge

- **silicon complexity**
  - impact of process scaling and new materials and architectures
  - previously ignorable phenomena now have impact

- **system complexity**
  - reuse
  - verification and test
  - cost-driven design optimization
  - embedded software design
  - reliable implementation platforms
  - design process management

- together: *superexponentially increasing complexity* of the design process
Methodology Precepts

ITRS

- exploit reuse
- evolve rapidly
- avoid iteration
- replace verification by prevention
- improve predictability
- orthogonalize concerns
- expand scope
- unify
Embedded System Design Challenges

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Overview of the Course
IP
- IP = Intellectual Property
- HW or SW block
- designed for reuse
- need of standards (VSIA)

platform based SoC design
- organized method
- to reduce cost and risk
- by heavy reuse of HW and SW IPs

steps in reuse
- block → IP → integration architecture
Raising the Abstraction Level

- **ESL** (Electronic System Level)
  - from RTL to TLM or higher
  - from VHDL to SystemC to UML

- **HW/SW co-design**
  - need new tools
  - consider the whole system
  - large optimization potential
  - combination of formal, semi-formal and non formal techniques
Other Problem: Power Consumption

Lower Bound for Fixed Chip Size
Power Consumption

- power consumption model

\[ \alpha CV_{dd}^2 f + I_{off} V_{dd} \]

- necessary improvement of power management (in 2016)
  - reduction by 20 for dynamic power
  - reduction by 800 for standby power

- one possible direction: exploit parallelism
  - allows to decrease \( f \)
  - and thus decrease \( V_{dd} \)
Summary

- challenge of SoC design
  - more complex
  - faster
  - cheaper
  - more reliable
  - with lower power consumption

- how to handle the complexity?
References

- *International Technology Roadmap for Semiconductors*
  - [http://public.itrs.net/](http://public.itrs.net/)
- *Winning the SoC Revolution*
  - Experiences in Real Design
  - Edited by Grant Martin & Henry Chang
  - Kluwer Academic Publishers
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Course Outline

- Embedded System Design Challenges (Pierre Boulet), 15 sept
- Codesign (Jean-Luc Dekeyser), 29 sept
- DaRT (Jean-Luc Dekeyser), 6 oct
- Models of Computation (Pierre Boulet), 13 oct
- MARTE UML profile (Pierre Boulet), 20 oct
- Model Driven Engineering (Anne Étien), 3 nov
- Validation (Abdoulaye Gamatié), 10 nov
- VHDL Synthezis (Philippe Marquet), 17 nov
- SystemC Simulation (Jean-Luc Dekeyser), 24 nov
- Applications (Jean-Luc Dekeyser et Frédéric Guyomarc’h), 1er déc
Course Evaluation

- research article synthesis
- exam