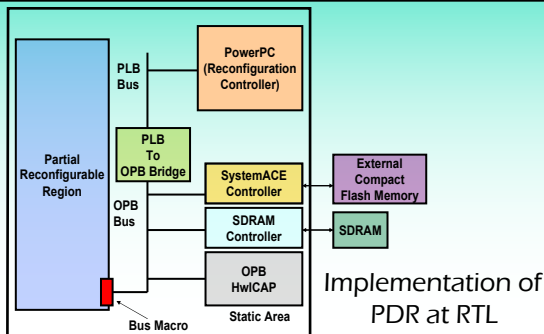


A MDE design flow for implementing Partially Dynamically Reconfigurable FPGAs

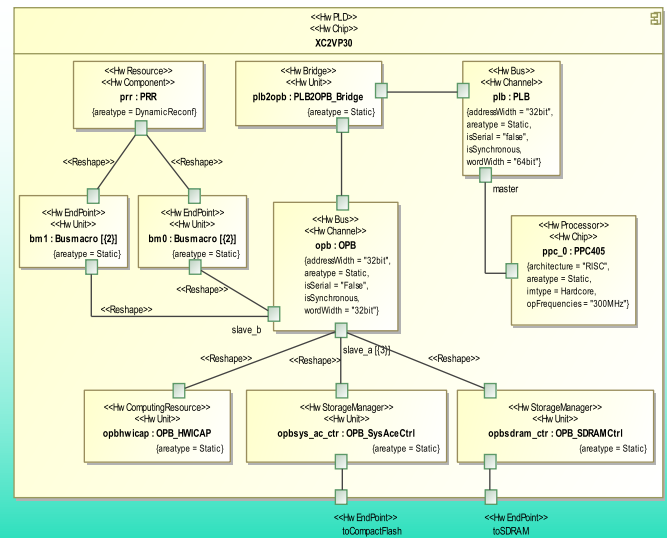
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Abstract : As System-on-Chip (SoC) design complexity continues to increase rapidly, new design methodologies are required to resolve this dilemma. In this paper we present a novel SoC co-design methodology based on Model Driven Engineering using the MARTE (Modeling and Analysis of Real-time and Embedded Systems) standard. We utilize this methodology to model fine grain reconfigurable architectures such as FPGAs and extend the standard to integrate new features such as Partial Dynamic Reconfiguration supported by modern FPGAs. The goal is to carry out modeling at a high abstraction level expressed in UML and following transformations of these models, automatically generate the code necessary for FPGA implementation.

1- FPGA architecture supporting PDR

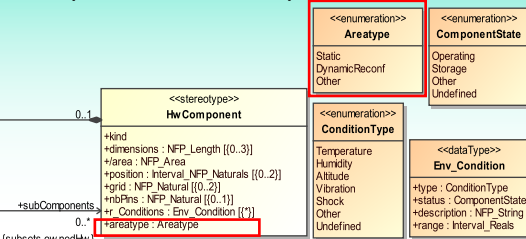


4- Modeling of a XC2VP30 chip



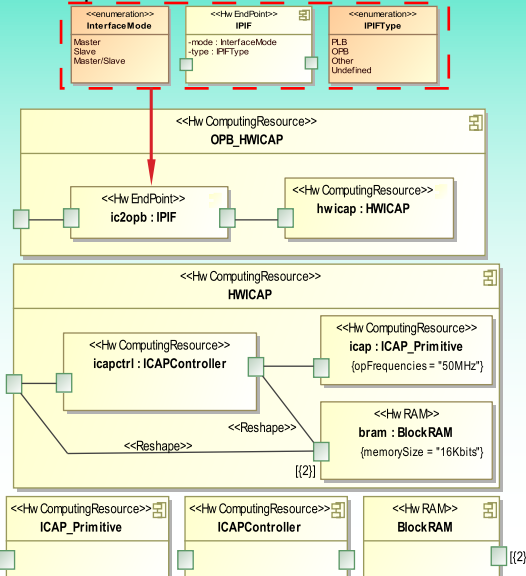
2- MARTE Modifications

Example of the HwComponent modification



3- Modeling of basic PDR concepts

Example of a Xilinx IPIF and OPBHWICAP



5- Case Study

Image Filter Task

