Dynamicity Analysis of Delta MINs for MPSOC Architectures

Yassine AYDI[1,2], Samy MEFTALI[2], Mohamed ABID[1], Jean-Luc DEKEYSER[2]
CES- National School of engineering of Sfax , Tunisia
LIFL and INRIA-Futurs, University of Lille, France
yassine.aydi@oous.rnu.tn, samy.meftali@lifl.fr , mohamed.abid@enis.rnu.tn, dekeyser@lifl.fr

Abstract

Multistage interconnection network has been very frequently proposed as connection means in classical on-board multiprocessor systems, it promises to be the solution for the interconnection problems. This paper tries to adapt such networks for embedded system design. Our approach is to analyze the dynamicity of the link permutation of Delta MINs for MPSOC architectures. This paper presents the design methodology and the performance evaluation of delta MINs.

SystemC timed simulations of the proposed MIN gives interesting results. These later should results derived from timing simulation are given. This study is to be used in future work in order to evaluate the NOC reconfigurability in which the connections change dynamically at run time.

Keywords

MPSOC, NOC, Delta MIN, Network design, Latency, Communication load.

1.Introduction

The new tendencies of microchip technologies envisage heterogeneous System on Chip (SoC) architectures consisting of complex integrated components communicating with each other at very high-speed rates, also they will have to be energy efficient, to handle nondeterministic applications and to provide sufficient processing capacity, all at the same time. Intercommunication requirements of future SoCs will not be feasible using a single shared bus or a hierarchy of buses due to their poor scalability with chip size and their shared bandwidth between all the components.

To overcome this problem, Network on Chip (NoC) has been proposed by academia and industry as a solution for the on-chip communication challenges for the future Multi processor system on chip denoted MPSoC architectures [1].

Multistage Interconnection Networks (MINs) are used in multi processors systems. As an example, MINs are frequently used to connect the nodes of IBMSP [2] and CRAY Y-MP series [3]. Further on, MINs are applied for Network on Chip to connect processors to memory modules on MPSOC [4].

Many variations of MINs have been introduced. These architectures provides a maximum bandwidth to components (processors, DSP, IP..), and minimum delay access to memory modules. A MIN is defined by: its topology, switching strategy, routing algorithm, scheduling mechanism [5], and fault tolerance [6].

The performance evaluation of the MIN is determined by modeling, using simulation [7], formal methods [8] or mathematical methods [9].

The major problems of the mathematic or formal method, is the complexity, the development time of a model, and the negligence of network parameters. Consequently, the performance results obtained by the model may become inaccurate. A simulation of a model is good opportunities to evaluate the performance of a MIN. Its advantages are a more detailed network description and a shorter time development. A dynamicity analysis of Delta MINs for MPSOC Architectures is investigated in this paper.

In section 2, the architecture of a multistage interconnection is introduced. Next, a design of a generic MIN and its components are presented. Section 3 gives a description for our evaluation strategy. Finally, simulation results and corresponding analyses are detailed.

2.MIN Basic

In this section we describe the MIN architecture that is used to design the interconnection platform dedicated for MPSOC.

We proposed in figure 1 a topological classification of MINs. They can be defined as a network used to interconnect a group of N inputs to a group of M outputs using several stages of switches elements led by linking stages [10].

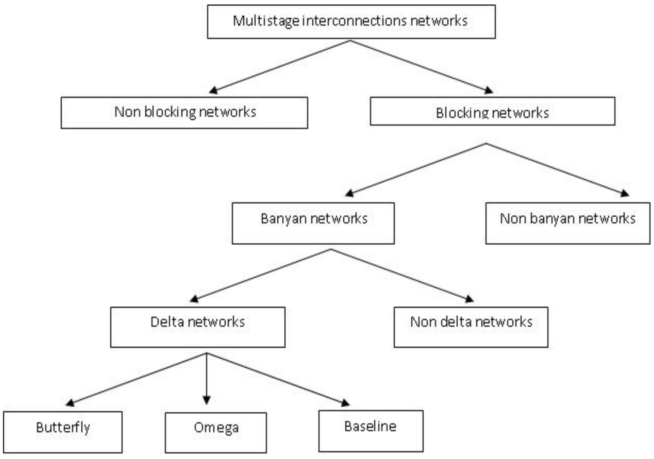

Fig.1: Classification of MINs

A. MINs with Banyan property

A banyan MIN is a multisatge interconnection network having the property of the existence of one and only one path between each source and destination.

For banyan MIN of size NxN consists of CxC crossbars, suppose that the switch input and output are presented to the base C (d_0 , d_1 , …..d_{c-1}) , and they have the same indexes, then digits d_0 of all inputs of a switch must be equal. A network having this characteristic is called to be having the Delta property [11].

B. MIN components

The basic building blocks of the MINs are switches elements, connected by links. The multistage networks having N inputs and N outputs nodes and using C×C switches have N/C number of switches at each stage. The number of nodes for K stages is N*K/2. Each stage is associated with a $\log_2 N$ bit vector called “stage-mask". A path between source and target is obtained by operating each corresponding switch in stage i in straight mode if the i bits of the source and the target are equals, otherwise in exchange mode.

3.Proposed MIN Platform

In this section, we present the MINs architectures designed for Multiprocessor System on Chip platform. The model of simulation is fully implemented in SystemC. It is preferred over a HDL language because of SystemC’s facility to model and simulate a large quantity of cycles and it has a high level descriptions as well as cycle-accurate precision. We define down the assumptions and the basic components under which our model is implemented and analyzed.

A. Network topology

The topology plays an important role in designing routing strategy, network latency, throughput and area.

We will restrict study to Delta MINs networks (figure 2). That is the MIN has N inputs and N outputs nodes using a switches elements which has C inputs and C outputs ports. There exist various popular MINs. The difference between each of these networks is the topology of interconnection links between the crossbar stages. A study of equivalence of various types of Delta MINs has been studied in [12].

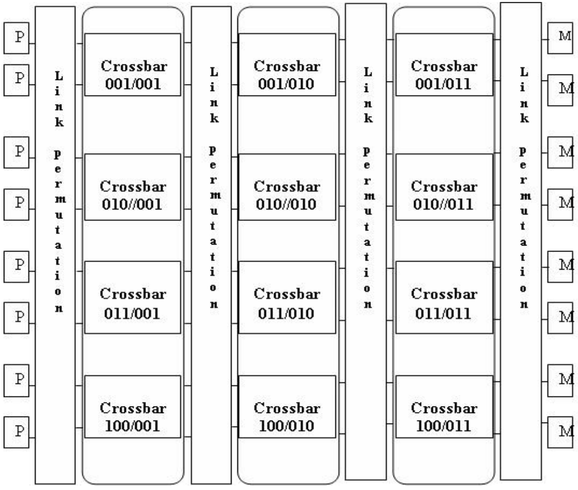

Fig.2: a generic model of a Delta MIN

We thus describe briefly the popular types of Delta MINs which has designed and analyzed:

-Omega networks: They use the identity permutation at the last stage and they use the perfect shuffle at all the others stages.

-Baseline networks: they use identity permutation at the first and the last stages and the rest are according to the baseline permutation. The ith baseline permutation performs a cyclic shuffling of the i + 1 least significant digits in the index to the right for one position.

-Butterfly networks: they are basically an unfolded hypercube. They use the identity permutation at the last stage, the perfect shuffle at the first stage and they use the butterfly permutation at all the others stages.

-Flip networks: they are a reverse image of Omega network.

B. Data exchanged

Traffic passed through the network is composed of fixed size packets. The switching strategy implemented requires dividing packets into flits, so the number of flits per packet is a parameter for simulation analysis.

The traffic is produced in sources, the bytes produced are driven by a random number generator, various offered load are introduced and analyzed for simulation. The targets represent the destination output, they are distributed uniformly, and they are in charge to remove the packets immediately upon arrival.

C. Buffer Sizing

Each one is connected to a input port of a switch, it store packets, it has a serious impact on the overall area. Various size of FIFO buffers are analyzed to evaluate the amount of buffering resources in the network architecture.

D. Router

Figure 3 shows the router designed with SystemC. It is composed of 2x2 crossbars, a control component (arbiter), a couple of input and output ports and a couple of FIFO connected to each input ports. The connection between the couple change dynamically according the destination in the packet header. The round robin algorithm stored in the arbiter is activated when multiple inputs contain messages routed to the same output. The switching processes also occur in every stage in pipeline.

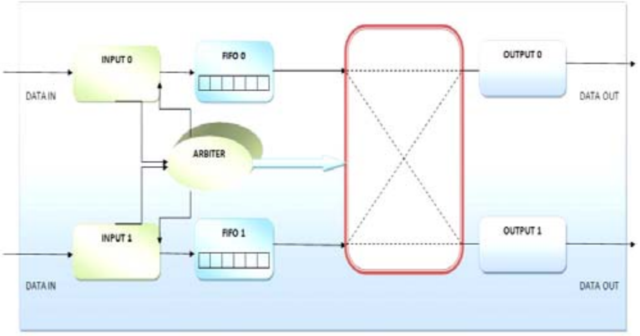

Fig.3: router's architecture

4. Evaluation strategy

The design of this model of simulation was driven by two goals. First, we evaluate and compare the affect of the link permutation of Delta MINs. Second, it should be able change connections dynamically at run time.

For evaluation performance, we define a communication scenario in witch traffic generated at source uniformly. Packets are generated at source; two sizes of packets are evaluated (16 and 32 bits). Sources and targets are selected randomly, and are injected at the packet header.

The routing between nodes is performed according to method proposed in the precedent section. The buffer size is a crucial parameter and it interacts with the performance parameters, the buffer size in the range of 1 to 5 packets are evaluated in the simulation.

We compare the performance of MINs having the same size of the switch elements to evaluate the dynamicity of the link permutation. Tested MINs are Omega, baseline, butterfly and flip networks.

The performance measures define a systematic decision for choosing the suitable Delta MINs for MPSOC architectures. We will limit our analysis to two parameters for performance evaluation: latency and communication management.

5.Simulation results

Simulations are run for Delta MINs have 8 inputs and 8 outputs nodes using a switches elements has 2 inputs and 2 outputs ports. All following figures identify the results derived from timing simulation. The latency is observed and managed by the GTKWave tool. First, traffic generators and crossbar elements are running at 1 GHz clock frequency as shown in figure 4.

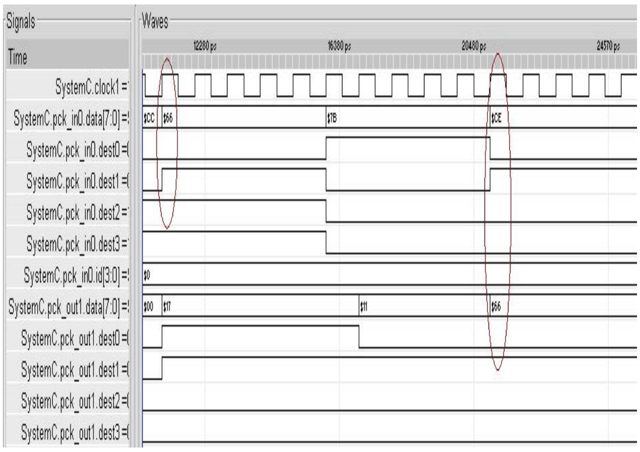

Fig.4: Latency measure with one clock

In second phase, we introduce a second clock to synchronize crossbar activities running three times more the first clock frequency, only traffic generators follow the first clock tick (figure 5) .

We deduce for the first implementation (only one clock) an average latency of network of 14ns, a rate of packets dropped of 48%. In the second model (two clocks), we measure an average latency of network of 5ns, a rate of packets dropped of 0% for the same duration of simulation.

Measurements obtained stimulated us for a model of simulation adapted to paradigm GALS (Globally Asynchronous, Locally Synchronous). Each subsystem (processors and network) follows its own clock tick.

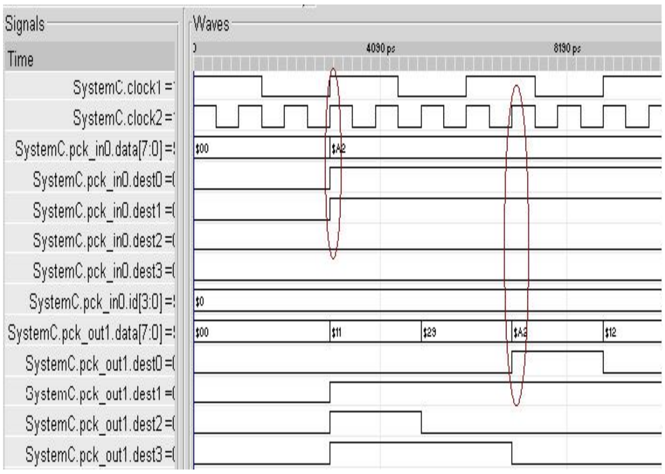

Fig.5: Latency measure with two clocks

A. *Buffer size evaluation*

Evaluating buffer size is a crucial work in switch design and has a serious impact on the overall area of the network. The figure 6 shows that the drop probability decreases as the buffer size increase for a heavy traffic, and it is slightly sensitive to Delta MINs type. For higher traffic, it is not significant that increasing buffer size decreases drop probability as shown in figure 7. We got the conclusion that buffer size is sensitive to communication load and dropped probability for a medium traffic network, and we estimate that the change of link permutation of Delta MINs dos not affect the choice of a reasonable buffer size.

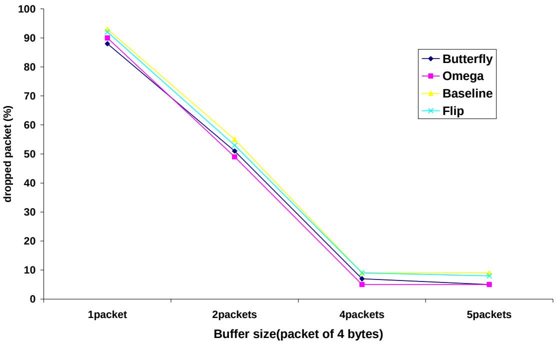

Fig.6: Dropped packets Vs Buffer size

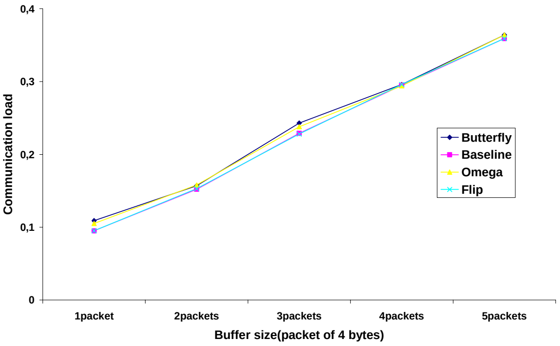

Fig.7: Communication load Vs Buffer size

B. *Communication load and drop probability*

The figure 8 shows that the drop probability increases as the communication load increases over some value of communication load. When communication load is less or equal than 0.16, the drop probability remains under 7%, which means the network has a light traffic and few packets are dropped. Also, we deduce that the rate of dropped packets is clearly different for all the type of Delta MINs simulated. We concluded that the drop probability is more sensitive to the communication load than to the buffer size and it is sensitive to the change of link permutation between switches elements.

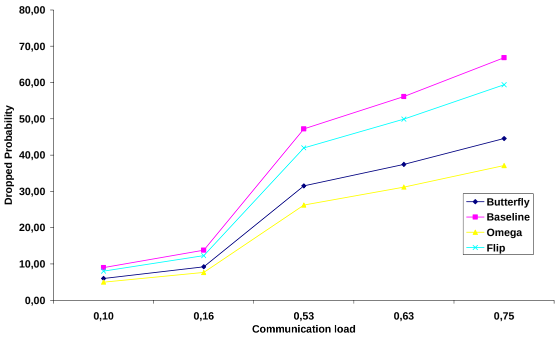

Fig.8: Communication load Vs Dropped packets

C. Network latency

The figure 9 shows that the average latency decreases as the buffer size increases. This can be explained as follow: it is evident when increasing buffer size, the probability of conflict to occur in switches decreases and message passes through networks quickly. Also, the same values of latency are obtained for different types of Delta MINs at all buffer sizes simulated. Finally, we concluded that changing connection between MINs stages does not affect latency.

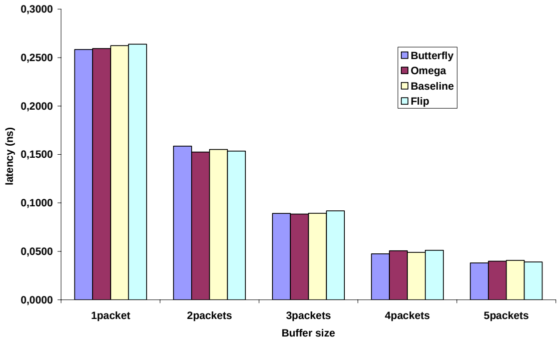

Fig.9: Latency Vs Buffer size

Conclusion and future work

MINs have been used as interconnection platform in multiprocessor systems. There exist various popular MINs. The difference between each of these networks is the link permutation between the crossbar stages. We proposed in this paper a model of simulation of a generic Delta MIN, developed using SystemC. For performance evaluation, we analyze same parameters in order to study the dynamicity of the link permutation of Delta MINs. This study is to be used in future work in order to evaluate the Delta MINs reconfigurability in which the connections change dynamically at run time.

References

[1] W.O. Cesario, "Multi-processor SoC platforms: a component-based design approach", IEEE Design and Test of Computers 19 (6) (2002), pp52–63.

[2] C. Stunkel, "The SP2 High-Performance Switch", IBM Systems Journal 34 (2) (1995), pp. 185–204.

[3] T. Cheung, "A simulation study of the cray x-mp memory system", IEEE Transactions on Computers 35 (7) (1986), pp613–622.

[4] S. Duquennoy, S. Le Beux , P. Marquet , S. Meftali , J. Dekeyser, "MpNOC Design: modeling and simulation", In 15th IP based SOC Design Conference (2006), pp229-232.

[5] C.P. Kruskal, "The performance of multistage interconnection networks for multiprocessors", IEEE Transactions on Computers 37 (11) (1986), pp1091–1098.

[6] C.C. Fan, J. Bruck, "Tolerating Multiple faults in Multistage interconnection Networks with Minimal Extra Stages", IEEE Transactions on Computers 49 (9) (2000), pp998–1004.

[7] D. Tutsch, M. Brenner, "MINSimulate . A Multistage Interconnection Network Simulator",. In 17th European Simulation Multiconference: Foundations for Successful Modeling & Simulation (ESM'03), Nottingham, pp 211.216.

[8] K. Goossens, "Formal Methods for Networks on Chips", In Fifth International Conference on Application of Concurrency to System Design :ACSD (2005), pp188-189.

[9] D. Tutsch, G. Hommel, "Generating Systems of Equations for Performance Evaluation of Buffered Multistage Interconnection Networks", Journal of Parallel and Distributed Computing 62 (2) (2002), pp228–240.

[10] T. Szymanski, V. Hamacher, "On the universality of multistage interconnection networks", *IEEE Computer Society Press* (1994) , pp. 73-101.

[11] C. Kruskal, M. Snir, "A unified theory of interconnection network ", Theoretical Computer Science 48 (1986), pp75-94.

[12] M. Collier, "A systematic analysis of Equivalence in Multistage Networks", In Journal of Light wave Technology 20 (9) (2002), pp228–240.